

Searching for **code marking and cache circuitry**.

Restrict to: Header Title Order by: Citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP

No documents match Boolean query. Trying non-Boolean relevance query.

1000 documents found. Only retrieving 250 documents (System busy - maximum reduced). Retrieving documents... Order: relevance to query.

[Interprocedural Array Data-Flow Analysis for Cache Coherence - Lynn Choi \(1995\)](#) (Correct) (1 citation)
 the inlining is often prohibitive due to both its **code** expansion and increase in its compilation time and boundary [5, 8] or inlining [8] to avoid reference **marking** interprocedurally. However, frequent **cache** Interprocedural Array Data-Flow Analysis for Cache Coherence Lynn Choi y Pen-Chung Yew Center
polaris.cs.uiuc.edu/reports/1427.ps.gz

[Using Virtual Lines to Enhance Locality Exploitation - Temam, Jegou \(1994\)](#) (Correct) (8 citations)
 Abstract Because the spatial locality of numerical **codes** is significant, the potential for performance improvements is important. However, large **cache** lines cannot be used in current on-chip **caches**
www.prism.uvsq.fr/archi/pubs/papers/TeJe94.ps.gz

[Optimizing ML with Run-Time Code Generation - Leone, Lee \(1995\)](#) (Correct) (91 citations)
 Optimizing ML with Run-Time **Code** Generation Mark Leone Peter Lee December 1995
foxnet.cs.cmu.edu/~petel/papers/staged/mleone-pldi96.ps

[Massively Parallel Computing: Mathematics and communications .. - Johnsson, Mathur \(1993\)](#) (Correct)
 59]In mature architectures, compiler generated **code** with supporting run-time systems achieves an of Technology, July 1986. 24] Geoffrey C. Fox, Mark A. Johnson, Gregory A. Lyzenga, Steve W. Otto, for such architectures. But, like for vector and **cache** based uniprocessor architectures, libraries, in
ftp.das.harvard.edu/techreports/tr-01-93.ps.gz

[Graphical Query Facility For Large Petri Net Simulation Runs - Oberweis, Sänger \(1992\)](#) (Correct)
 with petri nets means: starting with an initial **marking** of the net (an initial system state) one or more
aifbmozart.aifb.uni-karlsruhe.de/pub/INCOME-Project/saenger/EUROSIM92.ps

[Complementary Garbage Collector - Shogo Matsui](#) (Correct)
 of this algorithm in a parallel and an incremental **mark-sweep** GC indicate that it improves the efficiency
ftp.ml.info.kanagawa-u.ac.jp/pub/matsui/ComplementaryGC.ps.gz

[Foreign Event Handlers to Maintain Information Consistency and.. - Queloz \(1999\)](#) (Correct)
 paper is to describe novel applications of Mobile **Code** technology which have not appeared yet but should
cuiwww.unige.ch/~queloz/papers/mac3.1999.ps.gz

[A partial approach to the problem of deadlocks in.. - Tricas.. \(1998\)](#) (Correct)
 $X = S \times X \text{ ffl } X \times \text{ ffl } S \times X \times \text{ ffl } A$ **marking** is a mapping $M : P \setminus \Gamma \rightarrow \text{IN}$ in general, we
www.cps.unizar.es/~ftricas/GISIRR9705.ps.gz

[An Evaluation of Multiprocessor Cache Coherence Based on.. - Petersen, Li \(1994\)](#) (Correct) (8 citations)
 and invalidation instructions into application-**code**. The class of software coherence schemes we
 schemes. References AH90] Sarita V. Adve and Mark D. Hill. Weak Ordering -A new definition. In
 An Evaluation of Multiprocessor **Cache** Coherence Based on Virtual Memory Support Karin
sandbox.parc.xerox.com/petersen/ips94.ps.Z

[An Evaluation of a Compiler Optimization for Improving.. - Mounes-Toussi, Lilja, Li \(1994\)](#) (Correct)
 That is, for any two consecutive sections of **code** S1 and S2, if the write in S1 is immediately
 be written through to memory. These references are **marked** as not needing to send invalidation messages to
 mechanisms have been proposed for maintaining **cache** coherence in largescale shared-memory
ftp-mount.ee.umn.edu/pub/faculty/lilja/papers/reduced-inv-ics94.ps

[Computer Design Strategy for MCM-D/Flip-Chip Technology - Paul Franzon](#) (Correct)
 In the proposed organization, incoming **code** from the instruction **cache** is dynamically
 Thus there is tremendous advantage to building the **caches** in a computer in an SRAM process and using an MCM
 multiple entry points distributed over the IC **circuitry**, many more than would be available using

code marking and cache circuitry - ResearchIndex document query

www.ece.ncsu.edu/info.ece/vlsi_info/techreports/NCSU-ERL-96-03.PS.Z

Streamlining Data Cache Access with Fast Address Calculation - Austin, Pnevmatikatos, Sohi (1995) (Correct) (19 citations)

Abstract For many programs, especially integer **codes**, untolerated load instruction latencies account

Streamlining Data Cache Access with Fast Address Calculation Todd M.

<ftp.cs.wisc.edu/sohi/papers/1995/isca.fast.ps.gz>

Wrong-Path Instruction Prefetching - Pierce, Mudge (1994) (Correct) (16 citations)

prefetching does not help first-time accessed **code** since the table first needs to be set up with the
a grant from the Intel Corp. Abstract Instruction **cache** misses can severely limit the performance of both

www.eecs.umich.edu/techreports/cse/1994/CSE-TR-222-94.ps.gz

Cache Digests - Rousskov, Wessels (1998) (Correct) (47 citations)

or received with little or no gap (levels of line **markers** correspond to the number of digests transmitted

Cache Digests Alex Rousskov Duane Wessels National

www-sor.inria.fr/mirrors/wcw98/31/rousskov@nlanr.net.ps

Data and Computation Transformations for Multiprocessors - Anderson (1995) (Correct) (75 citations)

performance on modern architectures. Recent work on **code** transformations to improve **cache**
dimensions in the DISTRIBUTE statement that are not **marked** as "The folding functions map directly to
memory speeds is to employ one or more levels of **caches**. However, it has been notoriously difficult to
compiler.lcs.mit.edu/~saman/papers/anderson95.ps

An Extension of the Liveness Theory for Concurrent Sequential .. - Fernando Tricas (Correct)

ffl ut Proposition 2.2 (1)Let hN M 0 i be a **marked** ordinary Petri net. Let M 2 R(NM 0)be a

www.cps.unizar.es/~ftricas/SMC-95.ps.gz

Efficient Support for P-HTTP in Cluster-Based Web Servers - Aron, Druschel, Zwaenepoel (1999) (Correct) (9 citations)

(LARD)a content-based policy that achieves good **cache** hit rates in addition to load balance by

www.cs.rice.edu/~aron/papers/phhttp-lard.ps

Mechanisms and Interfaces for Software-Extended Coherent Shared.. - Chaiken (1994) (Correct) (3 citations)

little sensitivity to trap latency and memory system **code** efficiency, as long as they implement a minimum of
has already been achieved. Most workstation vendors **market** a product line that ranges from single-processor
ftp.cag.lcs.mit.edu/pub/papers/chaiken-dissert-1-10.ps.Z

Dynamic Access Ordering for Symmetric Shared-Memory Multiprocessors - McKee (1994) (Correct)

represent access patterns found in real scientific **codes**, including the inner-loops of blocked algorithms.

partitioned for a multiprocessor system can have a **marked** effect on performance. Three general scheduling

of memory components "on the other side of the **cache**" they should not be treated as uniform

ftp.cs.virginia.edu/pub/techreports/CS-94-14.ps.Z

Strategies for Representing Tone in African Writing Systems: A.. - Bird (1998) (Correct)

of new orthographies. One approach is to omit tone **marks**, just as stress is not **marked** in English (zero

www.ldc.upenn.edu/sb/papers/wll2/wll2.ps.Z

[First 20 documents](#) [Next 20](#)

Try your query at: [Amazon](#) [Barnes & Noble](#) [Google \(RI\)](#) [Google \(Web\)](#) [CSB](#) [DBLP](#)

CiteSeer - citeseer.org - [Terms of Service](#) - [Privacy Policy](#) - Copyright © 1997-2002 NEC Research Institute



Find: compiler and cacheability of code por

[Documents](#)[Citations](#)Searching for **compiler and cacheability w/2 code portions**.Restrict to: [Header](#) [Title](#) Order by: [Citations](#) [Hubs](#) [Usage](#) [Date](#) Try: [Amazon](#) [B&N](#) [Google \(RI\)](#) [Google \(Web\)](#) [CSB](#) [DBLP](#)**No documents match Boolean query. Trying non-Boolean relevance query.**1000 documents found. Only retrieving 250 documents (**System busy - maximum reduced**). Retrieving documents... Order: relevance to query.

[A short proof of Dirac's theorem on the number of edges..](#) - Deuber, Kostochka, Sachs (1996) (Correct)
www.mathematik.uni-bielefeld.de/stb343/preprints/pr96067.ps.gz

[Optimizing ML with Run-Time Code Generation](#) - Leone, Lee (1995) (Correct) (91 citations)

We describe the design and implementation of a **compiler** that automatically translates ordinary programs

[Optimizing ML with Run-Time Code Generation](#) Mark Leone Peter Lee December 1995
foxnet.cs.cmu.edu/~petel/papers/staged/mleone-pldi96.ps

[Uniform Reconstruction of Gaussian Processes](#) - Müller-Gronbach, Ritter (1995) (Correct) (1 citation)
ftp.math.fu-berlin.de/pub/math/publ/pre/1995/pr-a-95-26.ps.Z

[Effective Compiler Support for Predicated Execution..](#) - Mahlke, Lin, Chen, ... (1992) (Correct) (100 citations)

Effective Compiler Support for Predicated Execution Using the

basically replaces conditional branches in the **code** with comparison instructions which set a
cardit.et.tudelft.nl/~steven/ilp/mahlke92.ps.gz

[A Formal Compiler Specification Method](#) - Levin Boukimova (Correct)

A Formal **Compiler** Specification Method V. Levin, E.

power to treat contextual dependency of the target **code** on remotely distributed parts of the source **code**.
ftp.srdc.metu.edu.tr/pub/fmg/papers/a_formal_compiler_specification_method.ps.gz

[The System Of Two Spinning Disks In The Torus.](#) - Wojtkowski (1993) (Correct)
mpej.unige.ch/mp_arc/c/94/94-88.ps.gz

[Optimized Software Synthesis for Digital Signal..](#) - Jürgen Teich.. (1998) (Correct) (1 citation)

tolerability: in embedded DSP applications, **compilers** are allowed to spend more time for optimization

7.2.1.2 **Code** generation model .

ftp.tik.ee.ethz.ch/pub/people/zitzler/TZB1998a.ps.gz

[A generalized collision mechanism for stochastic particle..](#) - Rjasanow, Wagner (Correct)
www.wias-berlin.de/WIAS_publ_preprints_nr157.PS

[Identification Of Unknown Parameters For Heat Conductivity..](#) - Botkin (1995) (Correct)

www.appl-math.tu-muenchen.de/~botkin/hof444.ps

[The Jalapeño Dynamic Optimizing Compiler for Java](#) - Burke, Choi, Fink.. (1999) (Correct) (24 citations)

The Jalape~no Dynamic Optimizing **Compiler** for Java TM Michael G. Burke Jong-Deok Choi

www.mcs.newpaltz.edu/~hind/papers/grande99.ps

[An Integrated Compilation and Performance Analysis Environment for ..](#) - Adve (1995) (Correct) (30 citations)
 requires a unique degree of integration between **compilers** and performance analysis tools. **Compilers** for
vibes.cs.uiuc.edu/Publications/Papers/HPF.ps.gz

[Low Latency Word Serial CORDIC](#) - Villalba, Lang (1997) (Correct)
ftp.ac.uma.es/pub/reports/1997/UMA-DAC-97-05.ps.gz

[A Whole Sentence Maximum Entropy Language Model](#) - Rosenfeld (1997) (Correct) (4 citations)
 with virtually no change in the model or the **code**. 2 Throughout this paper we have been referring

www.cs.cmu.edu/afs/cs.cmu.edu/user/roni/WWW/rdi-IEEE-ASR97.ps

[A partial approach to the problem of deadlocks in..](#) - Tricas.. (1998) (Correct)
www.cps.unizar.es/~ftricas/GISIRR9705.ps.gz

compiler and cacheability w/2 code portions - ResearchIndex document query

Pitch Determination Considering Laryngealization.. - Niemann, Denzler, ... (1994) (Correct) (2 citations)

interpolate the F 0 -contour over laryngealized portions of speech. Figure 1 indicates that

www5.informatik.uni-erlangen.de/TeX/Literatur/ps-dir/1994/Niemann94.PDCa.ps.gz

Mechanisms and Interfaces for Software-Extended Coherent Shared.. - Chaiken (1994) (Correct) (3 citations)
about memory usage from the runtime system to the compiler. The compiler uses this information to optimize
little sensitivity to trap latency and memory system code efficiency, as long as they implement a minimum of
<ftp.cag.lcs.mit.edu/pub/papers/chaiken-dissert-1-10.ps.Z>

From System F to Typed Assembly Language - Morrisett, Walker, Crary, Glew (1998) (Correct) (4 citations)
the typing constructs admit most low-level compiler optimizations. Our translation to TAL is
a fully automatic way to produce proof carrying code, suitable for use in systems where untrusted and
www.cs.cmu.edu/~crary/papers/1998/tal/tal-long.ps.gz

The Stochastic Vortex Simulation of an Unsteady Viscous Flow .. - Szumbarski, Wald (1996) (Correct)
www.emath.fr/Maths/Proc/Vol.1/szumbars.ps

Development, Learning and Evolution in Animats - Kodjabachian, Meyer (1994) (Correct) (2 citations)
information on which the genetic algorithm operates codes for a set of production rules which are applied
www.biologie.ens.fr/fr/animatlab/perso/kodjaba/jkjamperac.ps.gz

Some properties of Fix-Free Codes - Ahlswede, Balkenhol, Khachatrian (Correct)
Some properties of Fix -Free Codes R.Ahlswede Fakultat fur Mathematik, Universitat
www.mathematik.uni-bielefeld.de/ahlswede/pub/balkenhol/fixfree.ps.gz

[First 20 documents](#) [Next 20](#)

Try your query at: [Amazon](#) [Barnes & Noble](#) [Google \(RI\)](#) [Google \(Web\)](#) [CSB](#) [DBLP](#)

CiteSeer - citeseer.org - [Terms of Service](#) - [Privacy Policy](#) - Copyright © 1997-2002 NEC Research Institute